PENDING CLAIMS

The following is a list of currently pending claims. Please amend claims 1-4 and 8-11 as shown below.

1. (Currently amended) An array of thin film transistors comprising polysilicon, wherein the polysilicon is formed by a method comprising:
   depositing a first layer of amorphous silicon;
   depositing silicon nuclei on the first layer of amorphous silicon;
   depositing a second layer of amorphous silicon over the first layer and the nuclei, wherein conversion of the first layer to hemispherical grains before deposition of the second layer is substantially prevented; and
   annealing the first and second layers of amorphous silicon to induce crystallization.

2. (Currently amended) The array of thin film transistors of claim 1, further comprising a charge storage region.

3. (Currently amended) The array of thin film transistors of claim 2, wherein the charge storage region is ONO-type.

4. (Currently amended) The array of thin film transistors of claim 2, wherein the charge storage region comprises a floating gate.

5. (Original) A monolithic three dimensional memory array comprising memory cells, said memory cells comprising polysilicon, any of said polysilicon crystallized by a method comprising:
   embedding deposited silicon nuclei between layers of amorphous silicon; and
   crystallizing from the embedded silicon nuclei.

6. (Original) The monolithic three dimensional memory array of claim 5, wherein the memory cells comprise TFTs.

7. (Original) The monolithic three dimensional memory array of claim 5, where the memory cells comprise antifuses and either diodes or diode components.

8. (Currently amended) An array of thin film transistors comprising a channel regions, the channel regions formed by a method comprising:

embedding deposited silicon nuclei between layers of amorphous silicon; and

annealing the nuclei and amorphous silicon layers.

9. (Currently amended) The array of thin film transistors of claim 8, each thin film transistor of the array further comprising a charge storage region.

10. (Currently amended) The array of thin film transistors of claim 9, wherein the charge storage region is ONO-type.

11. (Currently amended) The array of thin film transistors of claim 9, wherein the charge storage region comprises a floating gate.

CLAIM AMENDMENTS: DISCUSSION

Claims 1-4 and 8-11 were amended to refer to an *array* of transistors rather than to an individual transistor. Support for these claim amendments is found, for example, at paragraphs [0052]-[0054] of the present application. These amendments do not constitute new matter.